1. **SVA: ack must come after req, no ack without request.**  
   *bit past\_req;  
   always\_ff @(posedge clk) begin  
    if(req) past\_req<=1;   
    if(ack) past\_req <=0;  
   end  
   ap\_no\_req\_ack: assert property (@(posedge clk) !req && !ack);   
   ap\_req\_ack: assert property (@(posedge clock) req |-> past\_req ##[2:8] ack);*  
   // This was addressed before, but the same question keeps on arising.
2. **SVA in System Verilog to verify a signal switches from 0 to 1 prior to another signal's transition from 1 to 0**

*property sig\_a\_rises\_before\_sig\_b\_falls; @(posedge clk) disable iff (reset) (!sig\_a && sig\_b) |=> (sig\_a && sig\_b) ##[1:$] !$sig\_b; endproperty*

*assert property (@(posedge clk) disable iff (reset)*

*!$fell(sig\_b) |-> $rose(sig\_a)*

*);*

*3.*

*assert property (@(posedge clk) disable iff (reset)*

*$rose(sig\_a) ##[0:$] $fell(sig\_b)*

*);*

1. **Suppose there is another spec that says the following : -  
   1)There should be single gnt pulse for every req pulse made.  
   2)gnt can come between 1 to 100 clock cycle.  
   3)Its also possible that there can be another req pulse before the gnt of previous req pulse was completed (For example at time 0 there was req pulse and at time 3(say) there is another req pulse (till now there is no gnt for previous req pulses) so now if gnt comes it ,the following assertion would pass : -  
   req |-> ##[1:100] gnt.**

**One corner case scenario would be : - 10 req pulse came with single gnt (on say 11th cycle) but rest of the 9 gnts didn’t came.**

systemverilog

reg [31:0] req\_count, gnt\_count;

always @(posedge clk) begin

if (rst) begin

req\_count <= 0;

gnt\_count <= 0;

end else begin

if (req) req\_count <= req\_count + 1;

if (gnt) gnt\_count <= gnt\_count + 1;

end

end

property req\_gnt\_check;

@(posedge clk)

(req) |-> ##[1:100] (gnt && (req\_count == gnt\_count ));

endproperty

property req\_gnt\_eventual;

@(posedge clk)

(req\_count > gnt\_count) |-> ##[1:$] (gnt && (req\_count == gnt\_count));

endproperty

assert property (@(posedge clk) req\_gnt\_check);

assert property (@(posedge clk) req\_gnt\_eventual);

|  |  |  |  |
| --- | --- | --- | --- |
| S.no. | Property Description | Property | Comment |
| 1 | **SVA: ack must come after req, no ack without request.** | *bit past\_req; always\_ff @(posedge clk) begin  if(req) past\_req<=1;   if(ack) past\_req <=0; end ap\_no\_req\_ack: assert property (@(posedge clk) !req && !ack);  ap\_req\_ack: assert property (@(posedge clock) req |-> past\_req ##[2:8] ack);* // This was addressed before, but the same question keeps on arising. |  |
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